Gated Integrators and Boxcar Averagers

Model SR255 — 100 ps gated integrator

- **Gates of 100 ps, 200 ps, 500 ps & 1 ns**
- **Jitter <2 ps rms**
- **Droopless analog output**
- **Linear over full range**
- **20 ns insertion delay**
- **Trigger rates to 50 kHz**

SR255 Fast Sampler

The SR255 Fast Sampler module is a gated integrator with four discrete, user-selected gate widths from 100 ps to 1 ns. All of the necessary electronics are built into this high-speed module including an A/D, D/A and a PROM correction circuit to eliminate the inherent non-linearities in the sampling bridge.

The SR255 is perfect for fast pulsed experiments where the 2 ns minimum gate width of the SR250 is insufficient. The gate delay is controlled by a rear-panel voltage input which can be supplied by the SR200 Gate Scanner or the SR245 Computer Interface. Convenient gate view and signal outputs allow precise positioning of the gate—particularly important in applications such as time domain reflectometry or shorted-cable baseline subtraction. The SR255 can be used alone, combined with the SR245 Computer Interface module for automated data acquisition, or operated with the SR200 Gate Scanner for scanning gate waveform recovery.

Triggering

The SR255 has a DC-coupled trigger input (50 Ω) that supports trigger rates up to 50 kHz. The trigger threshold can be set to –0.5 V, +0.1 V or +1 V on the front panel. For reliable triggering, the trigger must remain over threshold for at least 5 ns, and not exceed 5 V.

Gate Delay

The delay from trigger to sample is controlled by an analog voltage applied at the rear of the unit. You can select delay ranges of 1, 10, 100 or 1000 ns/V with four switches accessed through the instrument's side panel. In addition to the adjustable delay, there is a fixed insertion delay of about 20 ns. With only 2 ps rms gate jitter, the SR255 makes it easy to set up and maintain precise gate timing.

Gate Width

Four fixed gate widths of 100 ps, 200 ps, 500 ps and 1000 ps can be selected. A front-panel LED indicates which gate width is being used.

Signal Input

The SR255 is designed to be used with RG58A cable. To achieve an optimally flat response, two meters of RG58A cable should be used with a BNC to N-Type converter (provided with each SR255). The frequency response of the SR255's front end has been peaked above 2 GHz to compensate for the losses in two meters of cable, and so this length of cable is recommended for the signal input line.

The signal input is passed to the signal out BNC via an internal 300 ps delay line. The signal output should be terminated in 50 Ω with a high quality terminator to minimize reflections and pulse distortion. The signal output aids in synchronizing the sample with the gate. The input signal should not exceed the sensitivity selection on the front panel, as the input is only protected to +5 VDC.

Gate View and Fast Timing

You can use the gate view output to time the sample gate with respect to the signal. The leading edge of the gate view output (50 ps rise time) indicates when the sample gate is being opened. The output is a pulse of approximately 3 V with an exponential decay of about 4 ns.

The sensitivity of the module (Vin/Vout) can be set to 1 V/V, 0.25 V/V or 0.1 V/V. For example, when 0.1 V/V sensitivity is selected, a 100 mV input will produce a 1 V output. The red overload LED will come on when the output exceeds 1 V.

Analog and Digital Outputs

The SR255 has both analog and digital outputs making it easy to interface in a wide range of experiments. The sample output provides a ±1 VDC full-scale analog voltage proportional to the value of the signal during the gate interval. Resolution is 0.5 % of full scale, and the output can drive up to 10 mA. This output is available 20 µs after the signal is sampled. Each unit is custom linearized with a PROM to ensure excellent linearity and full dynamic range.

Simple to Interface

The Fast Sampler also provides a digital interface through a 15-pin connector on the rear panel of the module. This interface is a parallel, binary interface which may be connected to either the 20-pin connector on the circuit board of the SR245 Computer Interface module or to any 8-bit digital I/O port.

The SR255 as a Sampling Scope

In this example, the SR255 is used with the SR200 Gate Scanner and an X-Y oscilloscope to provide sampling oscilloscope operation. A narrow gate is scanned over a repetitive waveform in order to recover its shape. A sampling "scope" made from the SR255 and SR200 can achieve 100 ps resolution at rates up to 50 ksamples/s.

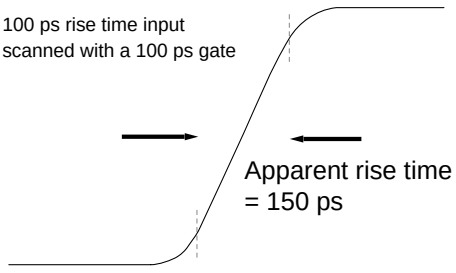
The SR200 is used to scan the gate delay over 0 to 10 times the selected delay scale. This scale is set on the SR255 to 1 ns, 10 ns, 100 ns or 1 µs to provide timebases with delays of up to 10 µs (100 µs w/ mod.). The X-AXIS OUT of the SR200 is used to drive the horizontal (X-axis) of the oscilloscope. The PEN LIFT OUT can be used to blank the CRT during retrace. The SAMPLE OUT of the SR255 is connected to the vertical (Y-axis) of the scope to display the sampled signal. Resolution is changed by changing the SR255's gate width.

Bandwidth and Noise

When looking at an infinitely fast edge, the apparent rise time is roughly equal to the selected gate width. The bandwidth of the unit is approximately equal to 0.35 divided by the gate width. The following table gives the available gate widths and corresponding bandwidth and noise.

Gate width	*Bandwidth*	*Noise (rms)*
1000 ps	350 MHz	200 mV
500 ps	700 MHz	350 mV
200 ps	1.7 GHz	600 mV
100 ps	3.5 GHz	800 mV

The figure below shows the measurement of a known 100 ps rise time edge using an SR255 "scope" with a 100 ps gate. We'd expect that the resultant pulse shape would be the convolution of the input signal with the SR255's gate. Since widths add roughly in quadrature under convolution, we'd



expect the observed rise time to be approximately $\sqrt{(100^2+100^2)}$ or 140 ps. The observed rise time is 150 ps.

From this discussion you might think that it's best to run with narrow gates to get the highest bandwidth and best step response. This is not necessarily the case. The penalty paid for using narrow gate widths is increased noise (see table above). Narrow gates have more noise because of their reduced sampling efficiency and wider bandwidth.

Gate Generator

Trigger in	
Termination	50 Ω
Thresholds	–0.5, +0.1 or +1 VDC
Trigger rate	DC to 50 kHz
Gate delay	20 ns + delay range × control voltage (Control input on rear)
Delay range	1, 10, 100 or 1000 ns/V
Gate jitter	<2 ps rms
Gate width	100, 200, 500, 1000 ps
Gate view	Leading edge indicates when gate opens (N-type connector)
Gate view accuracy	±50 ps with respect to signal out
Gate view rise time	<50 ps

Signal Channel

Signal In	Characteristic impedance is 50 Ω, protected to 5 VDC. The full-scale input level equals the sensitivity. setting. (N-Type connector)
Shot noise (typ.)	200 µV rms (1000 ps gate) 350 µV rms (500 ps gate) 600 µV rms (200 ps gate) 800 µV rms (100 ps gate)
Sensitivity	0.1, 0.25, or 1.0 V full scale Over range LED indicates signal greater than full scale.
Signal Out	The Signal In is passed to the Signal Out for termination, gate timing, etc. There is a 300 ps delay between Signal In and Signal Out.

Outputs

Sample Out	±1 V full-scale analog output. Linearized and latched representation of the signal input as sampled during the gate. Resolution is 0.5 % of full scale. Output impedance less than 1 Ω. 10 mA drive capacity.
Digital out	Rear-panel, 8-bit digital interface is addressed as two bytes: an 8-bit data byte for amplitude, an 8-bit status byte for sign, gate width sensitivity, data ready, rate error, and overrun status.

General

Power	+24 V/100 mA, –24 V/120 mA, +12 V/180 mA, approx. 8 watts
Connectors	Three N-type to BNC adapters are provided
Mechanical	Single-width standard NIM module
Warranty	One year parts and labor on defects in materials and workmanship

SR255 rear panel

Ordering Information

SR255 100 ps fast sampler